REMARKS

This responds to the Office Action mailed on April 9, 2008.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 38-43 are pending in this application.

§103 Rejection of the Claims

Claims 38-40 and 42-43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato (U.S. 6,124,725) in view of Gloudeman et al. (U.S. 6,119,125).

Claim 41 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato (U.S. 6,124,725) in view of Gloudeman et al. (U.S. 6,119,125) as applied to claim 38 above, and further in view of Ekstedt et al. (U.S. 5,206,582).

Sato discusses a system in which a switch mechanism switches between operation of an electric characteristic test mechanism and a reliability test mechanism such that the electric and reliability test mechanisms are sequentially coupled to the contactor (prober) when the contactor is in contact with a wafer under test.

Sato does not teach concurrent operation of semiconductor test equipment and parametric test instrumentation, as is recited in the pending claims, but instead teaches only sequential operation of various semiconductor test equipment.

Sato teaches throughout that only after the contactor is in contact with the wafer under test does Sato's switcher switch *sequentially* between an electric characteristic test mechanism and a reliability test mechanism (*see, e.g.,* the Abstract, ln. 13-18). Further, Sato's contactor 12 is cited as anticipating the claimed element of parametric test instrumentation, when a contactor or prober is defined in the pending application and claims as semiconductor test equipment.

The cited controller 35 is operable only to receive input from temperature sensors and control the temperature of the main chuck, and so also does not teach concurrent operation of semiconductor test equipment and parametric test instrumentation (*see,* col. 6, ln. 48-64).

Sato therefore fails to consider *concurrent* operation of semiconductor test equipment and parametric test instrumentation, as is recited in each of the pending claims.

Gouldeman nowhere contemplates semiconductor testing, and therefore also fails specifically to teach concurrent operation of semiconductor test equipment and parametric test instrumentation. Goundeman does discuss software components for a building automation system, including a simple finite state machine supporting a hierarchical state diagram, but again proceeds from one state to the next and does not suggest concurrency of any kind (*see, e.g.,* col. 17, ln. 39-46), much less concurrent operation of semiconductor test equipment and parametric test instrumentation to address the problems addressed by the claimed embodiments of the pending application.

Although Gouldeman addresses use of a finite state machine for building automation, it fails to teach a state oscillator module that controls the state of other modules, as is recited in the pending claims, particularly in the context of concurrent operation/control of semiconductor test equipment and parametric test instrumentation.

Moreover, the references cited are from different fields and provide no motivation to combine to address the present problem. The cited section of Gouldeman's col. 1, ln. 19-37 addresses avoiding hardware dependencies by providing software components that enable a systems integrator to configure a building automation system without worrying about the details of the underlying physical systems, which has little in common with operating semiconductor test and parametric test apparatus concurrently.

Should these rejections be maintained, applicant respectfully requests that it be pointed out specifically what elements of Sato and Goulderman are purported to anticipate concurrent operation of semiconductor test equipment and parametric test instrumentation and a state oscillator module that controls the state of other modules, so that applicant has an opportunity to expand on the differences between the references and what is claimed.

Because no part of Sato or Goulderman teaches concurrent operation of semiconductor test equipment and parametric test instrumentation or a state oscillator module that controls the state of other modules, the pending claims 38-43 appear to be in condition to be re-allowed. Reexamination and allowance of these pending claims is therefore respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 349-9581 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Aug 8 08 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 8th day of August, 2008.

Amy Moriarty
Name

Signature